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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,389	08/22/2000	Kevin K. Funk	10970997-3	8759

22878 7590 05/23/2003

AGILENT TECHNOLOGIES, INC.
INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT.
P.O. BOX 7599
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LOVELAND, CO 80537-0599

EXAMINER

VON BUHR, MARIA N

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



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2

Office Action Summary

Application No.

09/643,389

Applicant(s)

FUNK, KEVIN K.

Examiner

Maria N. Von Buhr

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. Examiner acknowledges receipt of Applicant's response to the previous Office action, received January 14, 2003; which submitted a declaration under 37 CFR §1.131. Claims 13-18 remain pending in this application.

2. In response to Applicant's above-noted declaration, submitted January 14, 2003, the 35 U.S.C. §102(a) and (e) rejections of claim 13, as being anticipated by the Kimura reference (Japanese Application No. 08-177051) and both of the Zvonar et al. references (U.S. Patent Nos. 5,942,739 and 5,828,989), respectively, and the 35 U.S.C. §103(a) rejections of claims 14-18, as being obvious over the Kimura reference (Japanese Application No. 08-177051) and both of the Zvonar et al. references (U.S. Patent Nos. 5,942,739 and 5,828,989), are deemed to have been overcome and are, therefore, withdrawn.

3. The finality of the previous Office action is withdrawn, in view of the new rejections of the claims presented below.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by Applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13-18 are rejected under 35 U.S.C. §102(b) as being clearly anticipated by Muraoka et al. (U.S. Patent No. 4,095,095), newly cited, which discloses "an apparatus for manufacturing semiconductor devices, particularly an apparatus which can control the manufacture of semiconductor devices by utilizing items of wafer processing information read out from patterns formed on the wafers to be used for manufacturing semiconductor devices" (col. 1, lines 5-10), wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly shown at least in Figure 6, and described at least at col. 1, line 32 - col. 2, line 10 and col. 4, lines 43 - col. 5, line 19. Muraoka et al. also clearly provide for their disclosed system being a "wafer stepper machine" by specifying the nature of the steps performed to form the semiconductor device at col. 6, lines 4-35.

6. Claims 13-18 are rejected under 35 U.S.C. §102(b) as being clearly anticipated by Fukasawa (U.S. Patent No. 4,930,086), newly cited, which discloses a method of stepwise manufacturing semiconductor devices, wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly shown at least in Figures 2 and 3, and described at least at col. 3, lines 30-40; col. 4, line 50 - col. 5, line 9; and col. 6, line 57 - col. 7, line 53.

7. Claims 13-18 are rejected under 35 U.S.C. §102(b) as being clearly anticipated by Barnett (U.S. Patent No. 5,432,702), newly cited, which discloses "a barcode processing system for a semiconductor wafer, comprising a workstation controller, a barcode reader attached to the workstation controller for reading a bar code assigned to the wafer, a tool assigned to the workstation controller for processing the wafer, and a host computer assigned to the tool and the workstation controller for determining the appropriate process to be performed on the wafer" (the abstract), wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly shown at least in Figures 1 and 2.

8. Claims 13-18 are rejected under 35 U.S.C. §102(a) as being clearly anticipated by Wu et al. (U.S. Patent No. 5,668,056), newly cited, which discloses "a manufacturing system for individually processing semiconductor wafers through a plurality of processing stations. the system has a plurality of processing stations, a multi-level track system that interfaces with the processing stations, and guided transport vehicles that operate on the track system to move individual wafers in wafer carriers between the stations. The carriers have a storage memory that contains the required process sequence and the capability to remember the completed process steps" (the abstract), wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly described at least at col. 1, lines 23-29; col. 2, line 61 - col. 3, line 62; col. 5, lines 30-58; col. 6, lines 53-61; col. 8, lines 22-50; col. 9, lines 3-11; and col. 10, lines 35-65.

9. Claims 13-18 are rejected under 35 U.S.C. §102(a) as being clearly anticipated by Asai et al. (U.S. Patent No. 5,692,292), newly cited, which discloses "a transfer type circuit board fabricating system having a plurality of working modules each including ... a working device for performing a predetermined operation on the circuit boards, and a controller constituted principally by a computer, for controlling the working device, ... the system further having a coordinating control device constituted principally by a computer,

for controlling the controllers of the working modules, on the basis of predetermined working schedule information stored therein" (the abstract), wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly shown at least in Figures 9 and 13-15, and described at least at col. 1, lines 6-16; col. 2, lines 26-67; col. 3, lines 25-47; col. 5, line 47 - col. 6, line 7; col. 18, line 62 - col. 19, line 17.

10. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 13-18 are rejected under 35 U.S.C. §103(a) as being obvious over Saka et al. (U.S. Patent No. 5,434,790), newly cited, which discloses "a versatile production system in which a communication-memory unit is attached to a product, ... while the product is conveyed along the production line. The communication-memory unit communicates with the line host controller via line terminals located at production line assembling and testing sites in order to send information relating to the product from the communication-memory unit to the line host controller ..." (the abstract), wherein the instantly claimed plural manufacturing machines with associated controllers, and human interface including display, scanning and control elements are clearly shown at least in Figures 1, 3 and 5. However, Saka et al. do not specify that the production system is necessarily one for manufacturing integrated circuit devices, including using wafer stepper and resist spin track machines, as instantly claimed. In this regard, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Saka et al. in the integrated circuit manufacturing environment, because Saka et al. teach a resultant benefit of versatility in manufacturing of the product, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

12. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

13. Any response to this Office action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to the Office at:

(703) 746-7239 - for formal communications intended for entry, mark "FORMAL";
(703) 746-7240 - for informal/draft communications; label "PROPOSED" or "DRAFT".

Hand-delivered papers should be brought to Crystal Park II, 2121 Crystal Dr., Arlington, VA, 4th Floor (Receptionist).

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Maria N. Von Buhr whose telephone number is (703) 305-3837. The Examiner can normally be reached on Monday-Friday between 9:00 A.M. and 5:00 P.M.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Leo Picard can be reached at (703) 308-0538.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.



MARIA N. VON BUHR
PRIMARY PATENT EXAMINER
ART UNIT 2125

MNVB
5/2/03